AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) In a network device, a central processing unit (CPU) comprising:

an arithmetic logic unit; and

a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations.

2. (original) The CPU of claim 1 wherein the one or more matching operations includes a network packet processing operation.

3. (original) The CPU of claim 2 wherein the packet processing operation includes an address lookup operation.

4. (original) The CPU of claim 3 wherein the address lookup operation includes an Internet Protocol (IP) address lookup operation.

5. (original) The CPU of claim 1 wherein the one or more matching operations includes a packet stuff/unstuff operation.

6. (original) The CPU of claim 1 wherein the one or more matching operations includes a packet classification operation.

7. (original) The CPU of claim 1 wherein the ternary content addressable memory is located within the arithmetic logic unit.

8. (original) The CPU of claim 1 further comprising:

a first register configured to store a first 32-bit operand; and

a second register configured to store a second 32-bit operand.

9. (currently amended) The CPU of claim 8 wherein the ternary content addressable memory performs the one or more matching operations based on at least one of the first [[and]] or second 32-bit operands.

10. (original) The CPU of claim 8 wherein the ternary content addressable memory includes a memory array including a group of 64-bit entries, and

wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand.

11. (original) The CPU of claim 1 wherein the ternary content addressable memory includes a memory array that includes a group of 64-bit entries.

12. (original) The CPU of claim 11 wherein the memory array comprises 32 entries.

13. (original) The CPU of claim 1 wherein, when performing the one or more matching operations, the ternary content addressable memory is configured to:

compare an operand to a group of entries.

14. (original) The CPU of claim 13 wherein the ternary content addressable memory is further configured to:

set a first flag when the operand fails to match an entry in the group of entries, and

set a second flag when the operand matches multiple entries of the group of entries.

15. (original) The CPU of claim 13 wherein, prior to comparing, the ternary content addressable memory is configured to:

sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory.

16. (currently amended) A method for processing packets in a network device, comprising:

receiving a packet; and

processing the packet using a ternary content addressable memory resident within ~~a processing~~ an arithmetic logic unit of the network device.

17. (canceled)

18. (original) The method of claim 16 wherein the processing includes performing a matching operation using information in a header of the packet.

19. (original) The method of claim 18 wherein the processing includes a packet classification operation.

20. (original) A system for forwarding packets in a network device, comprising:

means for receiving at least one packet; and

means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device.

21. (currently amended) An arithmetic logic unit comprising:

a register unit;

an operations unit; and

a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit.